

# Peripheral Interface Adapter (PIA)



## S6821/S68A21/S68B21

### Features

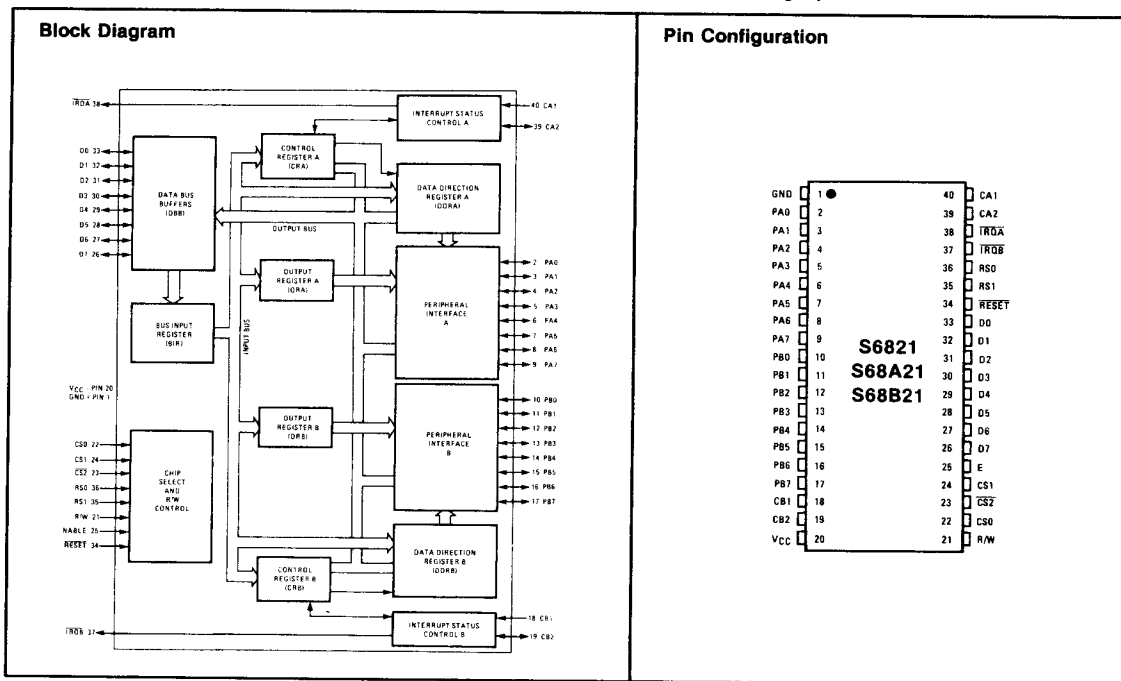
- 8-Bit Bidirectional Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

- Two TTL Drive Capability on all A and B Side Buffers
- TTL Compatible
- Static Operation

### General Description

The S6821/S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S6800/S68A00/S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the



S6800 FAMILY

## S6821/S68A21/S68B21

### General Description (Continued)

peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S6800/S68A00/S68B00 MPUs

with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with S6800/S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

### Absolute Maximum Ratings:

Symbol	Rating	Value	Unit
$V_{CC}$	Supply Voltage	-0.3 to +7.0	Vdc
$V_{IN}$	Input Voltage	-0.3 to +7.0	Vdc
$T_A$	Operating Temperature Range	0° to +70°	°C
$T_{stg}$	Storage Temperature Range	-55° to +150°	°C
$\theta_{ja}$	Thermal Resistance	82.5	°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

### Electrical Characteristics

$V_{CC} = 5.0V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0$  to 70°C unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
<b>Bus Control Inputs (R/W, Enable, Reset, RS0, RS1, CS0, CS1, CS2)</b>						
$V_{IH}$	Input High Voltage	$V_{SS} + 2.0$	—	$V_{CC}$	Vdc	
$V_{IL}$	Input Low Voltage	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc	
$I_{IN}$	Input Leakage Current	—	1.0	2.5	$\mu$ Adc	$V_{IN} = 0$ to 5.25 Vdc
$C_{IN}$	Capacitance	—	—	7.5	pF	$V_{IN} = 0$ , $T_A = 25^\circ\text{C}$ , $f = 1.0\text{MHz}$
<b>Interrupt Outputs (IRQA, IRQB)</b>						
$V_{OL}$	Output Low Voltage	—	—	$V_{SS} + 0.4$	Vdc	$I_{LOAD} = 3.2 \text{ mAdc}$
$I_{LOH}$	Output Leakage Current (Off State)	—	1.0	10	$\mu$ Adc	$V_{OH} = 2.4 \text{ Vdc}$
$C_{OUT}$	Capacitance	—	—	5.0	pF	$V_{IN} = 0$ , $T_A = 25^\circ\text{C}$ , $f = 1.0\text{MHz}$
<b>Data Bus (D0-D7)</b>						
$V_{IH}$	Input High Voltage	$V_{SS} + 2.0$	—	$V_{CC}$	Vdc	
$V_{IL}$	Input Low Voltage	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc	
$I_{TSI}$	Three State (Off State) Input Current	—	2.0	10	$\mu$ Adc	$V_{IN} = 0.4$ to 2.4 Vdc
$V_{OH}$	Output High Voltage	$V_{SS} + 2.4$	—	—	Vdc	$I_{LOAD} = -205 \mu\text{Adc}$
$V_{OL}$	Output Low Voltage	—	—	$V_{SS} + 0.4$	Vdc	$I_{LOAD} = 1.6 \text{ mAdc}$
$C_{IN}$	Capacitance	—	—	12.5	pF	$V_{IN} = 0$ , $T_A = 25^\circ\text{C}$ , $f = 1.0\text{MHz}$

## S6821/S68A21/S68B21

### Electrical Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions	
<b>Peripheral Bus (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)</b>							
$I_{IN}$	Input Leakage Current	R/W, Reset, RS0, CS0, CS1, CS2, CA1, CB1, Enable	1.0	2.5	$\mu$ Adc	$V_{IN} = 0$ to 5.25 Vdc	
$I_{TSI}$	Three-State (Off State) Input Current	PB0-PB7, CB2	2.0	10	$\mu$ Adc	$V_{IN} = 0.4$ to 2.4 Vdc	
$I_{IH}$	Input High Current	PA0-PA7, CA2	-200	-400	$\mu$ Adc	$V_{IH} = 2.4$ Vdc	
$I_{OH}$	Darlington Drive Current	PB0-PB7, CB2	-1.0	-10	mAdc	$V_O = 1.5$ Vdc	
$I_{IL}$	Input Low Current	PA0-PA7, CA2		-1.3	-2.4	mAdc	$V_{IL} = 0.4$ Vdc
$V_{OH}$	Output High Voltage	PA0-P7, PB0-PB7, CA2, CB2 PA0-PA7, CA2	$V_{SS} + 2.4$ $V_{CC} - 1.0$			Vdc $I_{LOAD} = -200\mu$ Adc $I_{LOAD} = -10\mu$ Adc	
$V_{OL}$	Output Low Voltage			$V_{SS} + 0.4$	Vdc	$I_{LOAD} = 3.2$ mAdc	
$C_{IN}$	Capacitance			10	pF	$V_{IN} = 0$ , $T_A = 25^\circ$ C, $f = 1.0$ MHz	
<b>Power Requirements</b>							
$P_D$	Power Dissipation			550	mW		

**A.C. (Dynamic) Characteristics** Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2 = 130pF and one TTL load for D0-D7, IRQA, IRQB ( $V_{CC} = 5.0V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0^\circ$ C to  $+70^\circ$ C unless otherwise specified)

**Peripheral Timing Characteristics:**  $V_{CC} - 5.0V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_A = 0^\circ$ C to  $+70^\circ$ C unless otherwise specified

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PDSU}$	Peripheral Data Setup Time	200		135		100		ns
$t_{PDH}$	Peripheral Data Hold Time	0		0		0		ns
$t_{CA2}$	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	$\mu$ s
$t_{RS1}$	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.50	$\mu$ s
$t_r, t_f$	Rise and Fall Times for CA1 and CA2 Input Signals	1.0		1.0		1.0		$\mu$ s
$t_{RS2}$	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	$\mu$ s
$t_{PDW}$	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	$\mu$ s
$t_{CMOS}$	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA0-PA7, CA2		2.0		1.35		1.0	$\mu$ s